R24 ACADEMIC REGULATIONS
COURSE STRUCTURE AND SYLLABI

of

M.TECH. VLSI DESIGN

FOR

M.Tech. REGULAR TWO YEAR DEGREE PROGRAM

(For the batches admitted from 2024-25)

CHOICE BASED CREDIT SYSTEM

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SRI VENKATESWARA COLLEGE OF ENGINEERING

(AUTONOMOUS)

(Affiliated to J.N.T. University Anantapur, Ananthapuramu, Accredited by NBA & NAAC "A")

Karakambadi Road, Tirupati - 517 507

Vision

To be a centre of excellence focusing on high quality technical education, research and technical services with global leadership competence to succeed in employment and higher education with ethical, social, entrepreneurial aspects updating to the real time requirements.

Mission

M 1: To impart high quality technical education by providing the state-of-the art infrastructure, core instruction.

M 2: Advanced research and technical consultancy services with qualified and senior faculty.

M 3: To prepare the students professionally deft and intellectually adept possessing excellent skill, knowledge and behavior with global competence.

Department of Electronics and Communication Engineering

Vision

To be a focal centre for Academic excellence in competing global standards and dynamics in the field of Electronics and Communication Engineering with research and services focusing on effective communication skills, entrepreneurial, ethical and social concern.

Mission

M 1: To impart quality technical education in Electronics and Communication Engineering with well established infrastructure, state-of-art laboratories core instructions and cognizant faculty.

M 2: To prepare the young and dynamic Electronics and Communication Engineers professionally deft and intellectually adept with knowledge, behavior and information competency.

M 3: To enable the learners for changing trends in the field of Electronics and Communication Engineering with a focus on career guidance, placements and higher education by industry institute relationship.

PROGRAM EDUCATIONAL OBJECTIVES

PEO1: Identify and apply appropriate design methods to solve problems in VLSI domain for developing innovative products and systems.

PEO2: Develop and apply suitable approaches in the domain of VLSI design to become a successful professional or an Entrepreneur.

PEO3: Pursue career in research in the domain of VLSI Design.

PROGRAM OUTCOMES

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

PROGRAM SPECIFIC OUTCOMES

PSO1: Attain, identify and apply knowledge of Physics of semiconductor devices and mathematics in VLSI design discipline to solve various engineering problems.

PSO2: Use techniques and modern CAD Tools so as to implement them in engineering practice to develop professional skills that will prepare them for immediate employment in industry.

PSO3: Analyze and design FPGA and ASIC based systems using industry standard tools

PRELIMINARY DEFINITIONS AND NOMENCLATURE

AICTE: Means All India Council for Technical Education, New Delhi.

Autonomous Institute: Means an institute designated as Autonomous by University Grants Commission (UGC), New Delhi in concurrence with affiliating University (**Jawaharlal Nehru Technological University Anantapur**).

Academic Autonomy: Means freedom to an institute in all aspects of conducting its academic programmes granted by UGC for promoting excellence.

Academic Council: The Academic Council is the highest academic body of theinstitute and is responsible for the maintenance of standards of instruction, education and examination within the institute. Academic Council is an authority as per UGC regulations and it has the right to take decisions on all academic matters including academic research.

Academic Year: It is the period necessary to complete an actual course of study within a year. It comprises two main semesters i.e., one odd and one even.

Branch: Means specialization in a programme like M.Tech degree programme in Computer Science and Engineering etc.

Board of Studies (BOS): BOS is an authority as defined in UGC regulations, constituted by Head of the Organization for each of the departments separately. They are responsible for curriculum design and updation in respect of all the programmes offered by a department.

Backlog Course: A course is considered to be a backlog course, if the student has obtained a failure grade in that course.

Commission: Means University Grants Commission (UGC), New Delhi.

Choice Based Credit System: It provides flexibility in designing curriculum and assigning credits based on the course content and hours of teaching along with provision of choice for the student in the course selection.

Continuous Internal Evaluation: It is an examination conducted towards sessional assessment.

Core: The courses that are the essential constituents of each engineering discipline are categorized as professional core courses for that discipline.

Course: A course is a subject offered by a department for learning in a particular semester.

Course Outcomes: The essential skills that need to be acquired by every student through a course.

Credit: A credit is a unit that gives weight to the value, level or time requirements of an academic course. The number of 'Contact Hours' in a week of a particular course determines its credit value. One credit is equivalent to one hour of teaching (Lecture / Tutorial) or two hours of practical work / field work per week.

Credit Point: It is the product of grade point and number of credits for a course.

Cumulative Grade Point Average (CGPA): It is a measure of cumulative performance of a student overall the completed semesters. The CGPA is the ratio of total credit points secured by a student in various courses in all semesters and the sum of the total credits of all courses in all the semesters. It is expressed up to two decimal places.

Curriculum: Curriculum incorporates the planned interaction of students with instructional content, materials and resources.

Department: An academic entity that conducts relevant curricular and co-curricular activities, involving both teaching and non-teaching staff, and other resources in the process of study for a degree.

Detention in a Semester: Student who does not obtain minimum prescribed attendance in a Semester shall be detained in that particular Semester.

Elective Course: A course that can be chosen from a set of courses. An elective can be Professional Elective and/or Open Elective.

Evaluation: Evaluation is the process of judging the academic performance of the student in her/his courses. It is done through a combination of continuous internal examinations and semester end examinations.

Grade: It is an index of the performance of the students in a said course. Grades are indicated by alphabets.

Grade Point: It is a numerical weight allotted to each letter grade on a 10 - point scale.

Institute: Represents **Sri Venkateswara College of Engineering, Tirupati** unless indicated otherwise by the context.

Massive Open Online Courses (MOOC): MOOCs inculcate the habit of self-learning. MOOCs would be additional choices in all the elective group courses.

Pre-requisite: A specific course or subject, the knowledge of which is required to complete before student register another course at the next grade level.

Professional Elective: It indicates a course that is discipline centric. An appropriate choice of minimum number of such electives as specified in the programme will leadto a degree with specialization.

Programme: Denotes PG degree programme: Master of Technology (M.Tech).

Dissertation / Project work: It is a design or research-based work to be taken up by a student duringhis/her final year to achieve a particular aim. It is a credit-based course and is to be planned carefully by the student.

Registration: Process of enrolling into a set of courses in a semester of a programme.

Regulations: The regulations, common to all M.Tech programmes offered by Institute, are designated as "SVCE – R24" and are binding on all the stakeholders.

Semester: It is a period of study with a minimum of 90 instructional days per semester (including all examinations). Each academic year of study is divided into two semesters.

Semester End Examinations: It is an examination conducted for all courses offeredin a semester at the end of the semester.

University: Represents Jawaharlal Nehru Technological University Anantapur (JNTUA), Ananthapuramu.

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1 General

1.1 About the College

Sri Venkateswara College of Engineering (SVCE) is part of the SV Colleges group established in the year 2007 with a vision to become a leader in providing quality educational services. College is affiliated to JNTUA & Approved by AICTE, recognized under sections 2(f) & 12(B) of UGC act 1956, Accredited by NAAC with 'A' Grade. Six B.Tech. Programmes CSE, ECE, EEE, IT, ME & CE are accredited by NBA, New Delhi. The College offers UG Programmes [CE, CSE, CSE (AI & ML), CSE (CS), CSE (DS), ECE, EEE, IT & ME], PG Programmes (VLSI Design, CSE, MCA & MBA). The Institution conferred 'Autonomy' by UGC, New Delhi in the year 2020.

The Campus is equipped with state of art laboratories of centre of excellence through advanced tools and technologies. Learning at Sri Venkateswara College of Engineering has a pragmatic approach with a clear focus, valuing individual vision, intellectual discipline, and a sense of teamwork. We aim at developing our students to their full potential, preparing them to take the next step towards career success.

Sri Venkateswara College of Engineering is committed to its role in creating leaders through its innovative programmes, outstanding faculty and thought leadership. Sri Venkateswara College of Engineering nurtures global leaders who can speak their minds and work well with others in a wide range of cultural contexts. It will develop their ability to manage a career successfully in the global economy.

Our teaching modes and methods of assessment vary between courses to ensure that you gain the most benefit from the interactive course content, faculty members, fellow students, and invited guests. Lectures comprise only a portion of course delivery, with the remaining taken up by discussions, seminars, case analysis, simulation, individual and group projects, and presentations.

Academic programmes of the College are governed by the rules and regulations as approved by the Academic Council, which is the highest academic body of the College. These academic rules and regulations are effective from the academic year 2024-25 for the students admitted into the two-year Post Graduate M.Tech. programme offered by the college.

1.2 Applicability

All the rules specified herein, approved by the Academic Council, shall be in force and applicable to students admitted from the academic year 2024–25 onwards. Any reference to 'College' in these rules and regulations stands for Sri Venkateswara College of Engineering.

1.3 Extent

All the rules and regulations, specified hereinafter shall be read as a whole for the purpose of interpretation and as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. It shall be ratified by the Academic Council in theforthcoming meeting. As per the requirements of statutory bodies, Principal, Sri Venkateswara College of Engineering shall be the Chairman, Academic Council.

1.4 Programmes Offered

Following programmes are offered in various branches in Sri Venkateswara College of Engineering leading to the award of M.Tech. Degree:

S No	Branch	Specialization	Branch Code
1	Electronics and Communication Engineering	VLSI Design	57
2	Computer Science and Engineering	Computer Science and Engineering	58

1.5 Semester System and Structure

A student after securing admission shall complete the M.Tech. programme in a minimum period of two academic years (4 semesters), and a maximum period of four academic years (8 semesters) starting from the date of commencement of first year first semester, failing which student shall forfeit seat in M.Tech. programme. Each semester shall normally consist of 90 instructional days having - Continuous Internal Evaluation (CIE) and Semester End Examination (SEE), Choice Based Credit System (CBCS) and Credit Based Semester

System(CBSS) as suggested by UGC and Curriculum/ Course Structure as suggested by AICTE/APSCHE are followed.

1.5.1 Semester Scheme

i. A Candidate after securing admission must pursue the M.Tech. programme of study for four semesters duration.
ii. Each Semester shall be of a minimum of 90 instructional days.
iii. A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.
iv. The medium of instruction of the programme shall be English only for all theory and practical courses, examinations, seminar, and project thesis/dissertation reports.

1.5.2 Course Classification

All courses offered for the post graduate programme in Engineering and Technology (M.Tech. degree programmes) are broadly classified as follows.

S. No.	Broad Course Classification	Course Group/ Category	Course Description	Credits
1	Core Courses	PC – Professional Core	Includes core courses related to the parent discipline/ department / branch of Engineering.	20
2	Elective Courses	PE – Professional Electives	Includes elective courses related to the parent discipline/ department / branch of Engineering.	18
3		OE – Open Electives	Elective courses which include interdisciplinary courses or courses in an area outside the parent discipline/ department/ branch of Engineering which are of importance in the context of special skill development.	
4	Research	Research Methodology and IPR	To understand importance and process of creation of patents through research	2
		TS - Technical Seminar	Seminar ensures preparedness of students to undertake major projects / dissertation, based on core contents related to parent discipline/ department/ branch of Engineering.	2
		Co-curricular Activities	Attending conferences, scientific presentations and other scholarly activities	2
		Project Work	M.Tech. Project Work or Major Project Work Phase - I and II	26
5	Mandatory Courses (MC)	Mandatory Non - Credit Courses	Covering courses of developing desired attitude and skills among the learners	NIL
6	Audit Courses (AC)	Audit Non - Credit Courses	Covering courses of developing desired attitude among the learners is on the line of initiatives such as Unnat Bharat Abhiyan, Yoga,	NIL

S. No.	Broad Course Classification	Course Group/ Category	Course Description	Credits
			Value education etc. Any other course helpful for enhancing the employability of the students.	
Total				**70**

- The college shall take measures to implement Virtual Labs (https://www.vlab.co.in) which provide remote access to labs in various disciplines of Engineering and will help student in learning basic and advanced concept through remote experimentation. Student shall be made to work on virtual lab experiments during the regular labs.
- A faculty advisor/mentor shall be assigned to each specialization to advise students on the programme, its Course Structure and Curriculum, Choice of Courses, based on his competence, progress, pre-requisites and interest.
- Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

1.6 Admissions

Admissions in to the first year of M.Tech. programme in Sri Venkateswara College of Engineering will be as per norms of Jawaharlal Nehru Technological University Anantapur, Ananthapuramu and Government of Andhra Pradesh.

Admissions shall be made either on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECET) for M.Tech. programmes/an entrance test conducted by University/on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

1.7 Award of M.Tech. Degree

A student will be declared eligible for the award of the M.Tech. degree if he/she fulfils the following:

1. Pursues a course of study for not less than two academic years and not more than four academic years.
2. Registers for 70 credits and secures all 70 credits.

Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M.Tech. programme and their admission stands cancelled.

2 Continuous Assessment

2.1 Attendance Requirement

i. A candidate shall be deemed to have eligibility to write Semester End Examinations if he/she has put in at least 75% of attendance on cumulative basis of all courses in the semester and 40% of minimum attendance should be maintained in each course.
ii. Condonation of shortage of attendance in aggregate upto 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee, if a student puts an aggregate attendance of 65% and minimum 40% in each course.
iii. Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence.
iv. A stipulated fee shall be payable towards condonation of shortage of attendance.
v. If the candidate does not satisfy the attendance requirement, he/she is detained for want of attendance and shall re-register for that semester. He/she shall not be promoted to the next semester. They may seek re-admission into that semester when offered next.
vi. If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

2.2 Choice Based Credit System (CBCS)

Choice Based Credit System (CBCS) is introduced in line with UGC guidelines in order to promote:

i. Student centered learning
ii. Students to learn courses of their choice
iii. Interdisciplinary learning

A Student has a choice of registering for courses comprising programme core,professional electives, open electives, MOOC courses, and courses related to research.

2.3 Evaluation

The performance of a student in each semester shall be evaluated course wise (irrespective of credits assigned), for a maximum of 100 marks for theory course and 100 marks for practical course, on the basis of Continuous Internal Evaluation and Semester End Examination.

For theory/practical courses the distribution shall be 40 marks for Continuous Internal Evaluation and 60 marks for the Semester End Examination.

2.3.1 Theory Courses

2.3.1.1 Continuous Internal Evaluation

For theory courses, during the semester, there shall be two midterm examinations, one in the middle of the semester and the other immediately after the completion of instructional period. First midterm examination shall be conducted for I, II units of syllabus. The second midterm examination shall be conducted for III, IV and V units. Each midterm examination shall be evaluated for 40 marks of which 30 marks for subjective paper (2-hour duration) and 10 marks for assignments.

Subjective paper shall contain 3 questions covering all the units of respective syllabus, student has to answer all the 3 questions, each question carries 10 marks.

***Note 1**: Any fraction shall be rounded off to the next higher mark.

If the student is absent for the midterm examination, no re-exam shall be conducted and midterm examination marks for that examination shall be considered as zero.

Final midterm examination marks shall be arrived at by considering the marks secured by the student in both the midterm examinations with 80% weightage given to the better midterm exam and 20% to the other.

2.3.1.2 Semester End Examination

End examination of theory courses shall have the following pattern:

i. There shall be 5 questions and all questions are compulsory.
ii. In each of the questions, there shall be either or type questions of 12 marks each from every unit of the syllabus. Student shall answer any one of them.
iii. Each question may consist of one, two or more bits

2.3.2 Practical Courses

For practical courses, 60 marks shall be for the Semester End Examinations and 40 marks will be for Continuous Internal Evaluation based on the day-to-day performance. The internal evaluation based on the day-to-day work - 10 marks, record - 10 marks and the remaining 20 marks to be awarded by conducting a midterm examination at the end of the instruction period. The Semester End Examination shall be conducted by the examiners, with a breakup mark of Procedure – 10 Marks, Experimentation – 25 Marks, Results - 10 Marks, Viva Voce - 15 Marks.

The laboratory records and midterm examination answer scripts shall be preserved for a minimum period of 3 years in the institute as per the norms and shall be produced to the Committees of the University as and when the same are asked for.

2.3.3 Project Work

The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters. Evaluation of Project work is for 300 marks with 200 marks for Continuous Internal Evaluation and 100 marks for Semester End Examination. Continuous Internal Evaluation of the Project Work Phase – I & Project Work Phase – II in III & IV semesters

respectively shall be for 100 marks each. Semester End Examination of final Project work viva voce in IV semester shall be for 100 marks.

A Project Evaluation Committee (PEC) shall be constituted with the Head of the Department, project supervisor, and project coordinator. The PEC is constituted by the Principal on the recommendations of the Head of the Department.

i. **Registration of Project Work**: A candidate is permitted to register for the Project Work in III Semester after satisfying the attendance requirement in all the courses, both theory and practical (in I & II semesters).
ii. The Project Work Phase – I shall be initiated in the third semester and the Project Work Phase – II will be continued in the final semester. The duration of the project work is for two semesters. The candidate can submit Project Thesis with the approval of PEC. The candidate has to pass all the theory, practical and other courses before submission of the Thesis.
iii. Project work shall be carried out under the supervision of teacher in the parent department concerned.
iv. A candidate shall be permitted to work on the project in an industry/research organization on the recommendation of the Head of the Department. In such cases, one of the faculty members from the department concerned would be the internal supervisor and an expert from the industry/ research organization concerned shall act as external supervisor. It is mandatory for the candidate to make full disclosure of all data/results on which they wish to base their Thesis. They cannot claim confidentiality simply because it would come into conflict with the Industry's or R&D laboratory's own interests. A certificate from the external supervisor is to be included in the Thesis.
v. Continuous Internal Evaluation of Project Work Phase - I and Project Work Phase – II in III & IV semesters respectively will be monitored by the PEC.
vi. The candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PEC before submission of the Project Thesis.
vii. After registration, a candidate must present in Project Work Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PEC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PEC can the student initiate the project work.
viii. The Project Work Review - II in III semester carries internal marks of 100. Evaluation should be done by the PEC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The PEC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work.
ix. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - II. Only after successful completion of Project Work Review – II, candidate shall be permitted for Project Work Review – III in IV Semester. The unsuccessful students in Project Work Review - II shall reappear for it as and when supplementary examinations are conducted.
x. The Project Work Review - III in IV semester carries 100 internal marks. Evaluation should be done by the PEC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PEC will examine the overall progress of the Project Work and decide whether or not eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Project Work Review - III after a month.
xi. For the approval of PEC the candidate shall submit the draft copy of Thesis to the Head of the Department and make an oral presentation before the PEC.
xii. After approval from the PEC, the students are required to submit a report showing that the plagiarism is within 30%. The Thesis report will be accepted only when the plagiarism is within 30%, which shall be submitted along with the Thesis report.

xiii. Research paper related to the Project Work shall be published in conference proceedings/UGC recognized journal. A copy of the published research paper shall be attached to the Thesis.
xiv. After successful plagiarism check and publication of research paper, three copies of the Thesis certified in the prescribed format given by the supervisor, shall be submitted to the HOD. One copy is to be forwarded to the controller of examinations and one copy to be sent to the external examiner.
xv. The HOD shall submit a panel of three experts for a maximum of **five** students at a time. However, the thesis will be adjudicated by one examiner nominated by the Principal.
xvi. If the report of the examiner is not satisfactory, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PEC. If report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the College.
xvii. If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva Voce exam.
xviii. The Project Viva Voce examinations shall be conducted by a board consisting of the Supervisor, Head of the Department and the External Examiner who has adjudicated the Thesis. For Thesis Evaluation (Viva Voce) in IV semester, there are external marks of 100 and it is evaluated by External Examiner. The candidate has to secure a minimum of 50% marks in Viva Voce exam.
xix. If he fails to fulfill the requirements as specified, he will reappear for the Project Viva Voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree.

2.3.4 Technical Seminar

There shall be a Technical Seminar for internal evaluation of 100 marks. A student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Seminar Evaluation Committee (SEC). Seminar Evaluation Committee shall be constituted with the Head of the Department, seminar supervisor, and seminar coordinator. The SEC is constituted by the Principal on the recommendations of the Head of the Department

The student has to secure a minimum of 50% of marks, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when supplementary examinations are conducted. The assessment of Technical seminar shall be conducted at the end of II semester instruction by SEC. There shall be no external examination for Technical Seminar.

2.3.5 Co-curricular Activities

The credits assigned for co-curricular activities shall be given by the Head of the Department and the same shall be submitted to the Principal. A Student shall earn 02 credits under the head of co-curricular activities, viz., attending Conference, Scientific Presentations and Other Scholarly Activities.

Following are the guidelines for awarding Credits for Co-curricular Activities

Name of the Activity	Maximum Credits/Activity
Participation in National level Seminar/Conference/ Workshops/ Training programs (Related to Specialization of the Student)	1
Participation in International Level Seminar / Conference / Workshop / Training programs (related to the specialization of the student)	2
Academic Award/Research Award from State Level/National Agencies	1
Academic Award/Research Award from International Agencies	2
Research / Review Publication in National Journals (Indexed in Scopus / Web of Science)	1
Research / Review Publication in International Journals with Editorial board outside India (Indexed in Scopus / Web of Science)	2

Note:

(i) Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit.

(ii) Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.

(iii) Participation in any activity shall be permitted only once for acquiring required credits under co-curricular activities.

2.3.6 Mandatory Courses

A candidate has to undergo 2 mandatory courses, which carries zero credits.

i. One mandatory course should be a theory course identified by the department, which will be evaluated for 40 marks of Continuous Internal Evaluation. A candidate has to secure a minimum of 50% of marks in the Continuous Internal Evaluation. A re-examination shall be conducted for failed students in the consecutive semester. There shall be no Semester End Examination. However, attendance in mandatory course shall be considered while calculating aggregate attendance in that semester.

ii. Another mandatory course is a MOOCs course to be done by the candidate as suggested by the department. The department shall give a list of standard MOOCs providers among Edx, Udacity, Coursera, NPTEL or any other standard providers with a minimum duration of not less than 8 weeks.

A student shall choose an online course (relevant to his/her programme of study)from the given list of MOOCs providers, with the approval of the HOD. If the student fails in completing the course with in the III semester, he/she must complete the course in the IV semester with the special permission from the Principal/Controller of Examinations.

2.3.7 Audit Courses

Audit courses carry "zero" credits. There shall be 1 audit course in II semester with no Continuous Internal Evaluation and Semester End Examination. However, attendance in audit courses shall be considered while calculating aggregate attendance in a semester. The student should study the audit course, and it shall be indicated in the grade sheet.

2.3.8 Summary - Distribution and Weightage of Marks

<table>
<tr><th>S No</th><th>Course</th><th>Marks</th><th colspan="3">Examination and Evaluation</th></tr>
<tr><td rowspan="3">1</td><td rowspan="3">Theory</td><td>60</td><td colspan="3">Semester End Examination for 3 hours duration</td></tr>
<tr><td rowspan="2">40</td><td>30</td><td colspan="2">Continuous Internal Evaluation (Two midterm examinations, each of 120 minutes duration)</td></tr>
<tr><td>10</td><td colspan="2">Average of two assignments, one assignment per each midterm examination</td></tr>
<tr><td rowspan="3">2</td><td rowspan="3">Laboratory</td><td>60</td><td colspan="3">Semester End Examination for 3 hours duration</td></tr>
<tr><td rowspan="2">40</td><td>20</td><td colspan="2">Regularity, viva, observation and record</td></tr>
<tr><td>20</td><td colspan="2">Internal exam</td></tr>
<tr><td rowspan="3">3</td><td rowspan="3">Project Work Phase - I and II</td><td rowspan="3">300</td><td rowspan="2">200</td><td>100</td><td>A report and presentation shall be made before PEC during Project Work Review - II in III semester of Project Work Phase - I.</td></tr>
<tr><td>100</td><td>A report and presentation shall be made before PEC during Project Work Review - III in IV semester of Project Work Phase - II.</td></tr>
<tr><td>100</td><td colspan="2">In Project Work Phase - II, if the report of the examiner is favourable, Viva Voce examination shall be conducted by the board, consisting of the Supervisor, Head of the Department and the External Examiner who adjudicated the Thesis.</td></tr>
</table>

S No	Course	Marks	Examination and Evaluation
4	Technical Seminar	100	A report and a presentation shall be made before a SEC.
5	Mandatory Theory Course	40	Continuous Internal Evaluation shall be conducted and evaluated similar to theory courses. There shall be no Semester End Examination. However, attendance in mandatory course shall be considered
	Mandatory MOOC Course	-	Student shall complete a certificate course offered by external agencies.
6	Audit Courses	-	There shall be no Continuous Internal Evaluation and Semester End Examination. However, attendance in audit course shall be considered

2.3.9 Re-Registration for Improvement of Continuous Internal Evaluation Marks

Following are the conditions to avail the benefit of improvement of Continuous Internal Evaluation Marks.

i. The candidate should have completed the course work and obtained examinations results for **I, II and III** semesters.
ii. He / She should have passed all the courses for which the Continuous Internal Evaluation marks secured are more than 50%.
iii. Out of the courses the candidate has failed in the examination due to Continuous Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory courses and for a maximum of **three** Theory courses for Improvement of Continuous Internal Evaluation marks.
iv. The candidate has to re-register for the chosen courses before the start of the semester in which re-registration is required and fulfil the academic requirements.
v. For each re-registered course, the candidate has to pay a prescribed fee.
vi. In the event of availing the Improvement of Continuous Internal Evaluation marks, the Continuous Internal Evaluation marks as well as the Semester End Examinations marks secured in the previous attempt(s) for the re-registered courses stand cancelled.

2.3.10 Recounting / Revaluation

Students shall be permitted to apply for Recounting / Revaluation of the Semester End Examination answer scripts against notification within a stipulated period, after payment of the prescribed fee. After completion of the process of Recounting / Revaluation, the records are updated with changes if any, and the student shall be issued a revised grade sheet. If there are no changes, the student shall be intimated the same through a notice.

The Revaluation shall be carried out by an expert not less than Associate Professor cadre, as per the scheme of evaluation supplied by the examination branch in the presence of Principal / Controller of Examinations. Neither the students nor his parents shall be permitted to be present during the valuation.

2.3.11 Supplementary Examinations

In addition to the regular Semester End Examinations conducted, the college may also schedule and conduct supplementary examinations for all the courses of other semesters when feasible for the benefit of students. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

2.3.12 Withholding of Results

In case of indiscipline or malpractice is pending against a candidate, the result of the candidate shall be withheld and he/she shall not be allowed/promoted to the next higher semester.

2.4 Credit Transfer Policy

As per University Grants Commission (Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016, the Institution shall allow up to 40% of the total courses being offered in a particular Programme in a semester through the Online Learning courses through SWAYAM.

i. The institution shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM platform.
ii. The online learning courses available on the SWAYAM platform will be considered for credit transfer. SWAYAM course credits are as specified in the platform.
iii. Student registration for the MOOCs shall be only through the department, it will be mandatory for the student to share necessary information with the department.
iv. The list of MOOCs shall be identified, approved and notified by the Head of the Department.
v. The department shall select the courses to be permitted for credit transfer through SWAYAM. However, while selecting courses in the online platform department would essentially avoid the courses offered through the curriculum in the offline mode.
vi. The department shall notify at the beginning of semester; the list of the online learning courses eligible for credit transfer in the forthcoming semester.
vii. The department shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester.
viii. The department shall designate a faculty member as a mentor for each course to guide the students from registration till completion of the credit course.
ix. The institution shall ensure no overlap of SWAYAM MOOC exams with that of the Semester End Examination schedule. In case of delay in SWAYAM results, the Institute will re-issue the marks sheet for such students.
x. Student pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the percentage of marks and grades.
xi. The department shall submit the following to the examination section of the institution:
    a) List of students who have passed MOOC courses in the current semester along with the certificates of completion.
    b) Undertaking form filled by the students for credit transfer.
xii. The Institution shall resolve any issues that may arise in the implementation of this policy from time to time and shall review its credit transfer policy in the light of periodic changes brought by UGC, SWAYAM, NPTEL and State government.

Note: Students shall also be permitted to register for MOOCs offered through online platforms other than SWAYAM NPTEL. In such cases, credit transfer shall be permitted only after seeking approval of the Institution at least three months prior to the commencement of the semester.

2.5 Student Transfers

Student transfers shall be as per the guidelines issued by the Government of Andhra Pradesh from time to time.

3 Grading System

3.1 Credits

A credit is a unit that gives weight to the value, level or time requirements of an academic course. The number of 'Contact Hours' in a week of a particular course determines its credit value. One credit is equivalent to one hour of teaching (Lecture / Tutorial) or two hours of practical work / field work per week.

All courses are to be registered by the student in a semester to earn credits which shall be assigned to each course in an L T P C (Lecture Periods; Tutorial Periods; Practical Periods; Credits) structure based on the following general pattern.

Particulars	No. of Credits
1 Hour Lecture (L) per week	1
1 Hour Tutorial (T) per week	1
1 Hour Practical (P) per week	0.5
2 Hours Practical (P) per week	1
Technical Seminar	2

Dissertation / Project Work	26
Mandatory Courses/Audit Courses	0

3.1.1 Total Credits

The curriculum is designed for M.Tech. programme so that the total credits will be 70. To become eligible for the award of degree, every student shall earn all the credits of 70 specified in the curriculum of the programme.

3.2 Award of Grades

As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed:

After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.

Range in which the Marks in the Course fall	Grade	Grade points Assigned
≥ 90	S(Superior)	10
≥ 80 < 90	A (Excellent)	9
≥ 70 < 80	B (Very Good)	8
≥ 60 < 70	C (Good)	7
≥ 50 < 60	D (Average)	6
< 50	F (Fail)	0
Absent	Ab (Absent)	0

A student obtaining Grade 'F' or Grade 'Ab' in a course shall be considered failed and will be required to reappear for that course when it is offered in the next supplementary examination.

3.2.1 Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA)

i. The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.

$$SGPA = \sum_{i=1}^{n}(C_i \times G_i) \Big/ \sum_{i=1}^{n} C_i$$

Where, C_i is the number of credits of the i^{th} course, G_i is the grade point scored by the student in the i^{th} course and n is the number of courses.

ii. The Cumulative Grade Point Average (CGPA) will be computed in the same manner taking into account all the courses undergone by a student in all the semesters of a programme, i.e.

$$CGPA = \sum_{i=1}^{n}(C_i \times S_i) \Big/ \sum_{i=1}^{n} C_i$$

Where S_i is the SGPA of the i^{th} semester, C_i is the total number of credits up to thatsemester and n is the number of semesters.

iii. Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

iv. While computing the SGPA, the courses in which the student is awarded Zero grade points will also be included.

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale.

Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D, and F.

3.3 Award of Degree and Class

A candidate shall be eligible for the award of M.Tech. degree if he/she satisfies the minimum academic requirements prescribed for the completion of the programme, he/she shall be placed in one of the following three classes, based on overall CGPA obtained.

Class Awarded	CGPA Secured
First class with Distinction	≥8
First class	<8 and ≥7
Pass class	<7 and ≥6

4. Exit Policy

The student shall be permitted to exit with a PG Diploma based on his/her request to the institution through the department at the end of first year subject to passing all the courses in first year.

The institution shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE and State government.

5. Transitory Regulations

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfillment of academic regulations. Candidates who have been detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent courses as and when courses are offered, subject to Section 1.6 and they will follow the academic regulations into which they are readmitted.

6. General Instructions

i. The academic regulations should be read as a whole for purpose of any interpretation.
ii. Rules for disciplinary action for malpractice / improper conduct in examinations are appended.
iii. Where the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers", respectively.
iv. In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.

7. Amendments to Regulations

The Academic Council of Sri Venkateswara College of Engineering (Autonomous) reserves the right to revise, amend, or change the Regulations, Scheme of Examinations, and / or Syllabi or any other policy, depending on the relevant needs of the society or industrial requirements etc., with the recommendations of the concerned Board(s) of Studies. The amendments shall be made applicable to all the students on rolls with effect from the dates notified by the institution.

NOTE: FAILURE TO READ AND UNDERSTAND THE RULES & REGULATIONS IS NOT AN EXCUSE

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8 RULES FOR DISCIPLINARY ACTION FOR MALPRACTICE / IMPROPER CONDUCT INEXAMINATIONS

	Nature of Malpractices / Improper conduct	**Punishment**
	If the candidate:	
1 (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the course of the examination)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or Outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the notice of Principal.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from Class work and all Semester End examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the courses of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that semester/year. The candidate is also debarred for four consecutive semesters from class work and all Semester End Examinations if his involvement is established. Otherwise, the candidate is debarred for two consecutive semesters from class work and all Semester End Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

	Nature of Malpractices / Improper conduct	**Punishment**
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all Semester End Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course only.
6	Refuses to obey the orders of the Chief Superintendent /Assistant - Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that semester/year. If the candidate physically assaults the invigilator / officer-in-charge of the Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all Semester End Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

	Nature of Malpractices / Improper conduct	**Punishment**
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred and forfeits the seat. Person (s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that course only or in that course and all other courses the candidate has appeared including practical examinations and project work of that semester / year examinations, depending on the recommendation of the committee.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Principal for further action to award suitable punishment.	

Note: Whenever the performance of a student is cancelled in any course(s) due to Malpractice, he/she has to register again for Semester End Examinations in that course(s) consequently and has to fulfill all the norms required for the award of Degree.

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COURSE STRUCTURE

I Semester

S. No	Course Code	Course Name	Contact Periods per Week				Credits	Scheme of Examination Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1	EC24DPC101	CMOS Analog IC Design	3	0	0	3	3	40	60	100
2	EC24DPC102	CMOS Digital IC Design	3	0	0	3	3	40	60	100
3	EC24DPE101 EC24DPE102 EC24DPE103	**Program Elective Course I** CAD for VLSI Hardware for Deep learning Microchip Fabrication Techniques	3	0	0	3	3	40	60	100
4	EC24DPE104 EC24DPE105 EC24DPE106	**Program Elective Course II** ASIC Design CPLD and FPGA Architectures and Applications Organic Electronics	3	0	0	3	3	40	60	100
5	EC24DRM101	Research Methodology and IPR	2	0	0	2	2	40	60	100
6	EC24DPC103	CMOS Analog IC Design Lab	0	0	4	4	2	40	60	100
7	EC24DPC104	CMOS Digital IC Design Lab	0	0	4	4	2	40	60	100
8	EC24DMC101	**Mandatory Course** Entrepreneurship and Incubation	2	0	0	2	0	40	--	40
Total			**16**	**0**	**8**	**24**	**18**	**320**	**420**	**740**

II Semester

S. No	Course Code	Course Name	Contact Periods per Week				Credits	Scheme of Examination Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1	EC24DPC201	CMOS Mixed Signal Design	3	0	0	3	3	40	60	100
2	EC24DPC202	Physical Design Automation	3	0	0	3	3	40	60	100
3		**Program Elective III**	3	0	0	3	3	40	60	100
	EC24DPE201	MEMS System Design								
	EC24DPE202	Semiconductor Memory Design and Testing								
	EC24DPE203	VLSI test and testability								
4		**Program Elective IV**	3	0	0	3	3	40	60	100
	EC24DPE204	Biomedical CMOS IC's								
	EC24DPE205	Electronic Packaging and 3D IC Technologies								
	EC24DPE206	VLSI Signal Processing								
5	EC24DPC203	Mixed Signal IC Design Lab	0	0	4	4	2	40	60	100
6	EC24DPC204	Physical Design Automation Lab	0	0	4	4	2	40	60	100
7	EC24DTS201	Technical Seminar	2	0	0	2	2	100	--	100
8		**Audit Course**	2	0	0	2	0	--	--	--
	EG24DAC201	English for Research Paper Writing								
Total			**16**	**0**	**8**	**24**	**18**	**340**	**360**	**700**

III Semester

S. No	Course Code	Course Name	Contact Periods per Week				Credits	Scheme of Examination Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1	EC24DPE301 EC24DPE302 EC24DPE303	**Program Elective III** Bi-CMOS Technology and Applications Optimization Techniques and Applications in VLSI Design System on Chip Architecture	3	0	0	3	3	40	60	100
2	EC24DOE301 EC24DOE302 EC24DOE303 EC24DOE304	**Open Elective** Embedded System Design Foundations of Artificial Intelligence Introduction to Industry 4.0 and Industrial Internet of Things Natural Language Processing	3	0	0	3	3	40	60	100
3	EC24DCA301	Co-curricular Activities	0	0	0	0	2	--	--	--
4	EC24DMC301	MOOCS (Mandatory Course)	0	0	0	0	0	--	--	--
5	EC24DPR301	Project Work Phase - I	0	0	20	20	10	100	--	100
Total			**6**	**0**	**20**	**24**	**18**	**180**	**120**	**300**

IV Semester

S. No	Course Code	Course Name	Contact Periods per Week				Credits	Scheme of Examination Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1	EC24DPR401	Project Work Phase - II	0	0	32	32	16	100	100	200
Total			**0**	**0**	**32**	**32**	**16**	**100**	**100**	**200**

M.Tech. – I Semester

L	T	P	C
3	0	0	3

(EC24DPC101) CMOS ANALOG IC DESIGN

COURSE OBJECTIVES:

The objective of this course are to:

- Focus on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
- Basic design concepts, issues and trade-offs involved in analog IC design are explored.
- Intuitive understanding and real-life applications are emphasized throughout the course.
- Learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage OpAmps, Cascade Op Amps, Measurement Techniques of OP Amp.
- Know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Design MOSFET based analog integrated circuits.
CO 2: Analyze analog circuits at least to the first order.
CO 3: Appreciate the trade-offs involved in analog integrated circuit design.
CO 4: Understand and appreciate the importance of noise and distortion in analog circuits.
CO 5: Analyze complex engineering problems critically in the domain of analog ICdesign for conducting research.

Unit I: (10 Periods)

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS Devicemodels. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

Unit II: (8 Periods)

Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active CurrentMirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.

UNIT III: (10 Periods) Frequency

Response of Amplifiers: General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT IV: (10 Periods)

Feedback Amplifiers: General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps,Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation.

UNIT V: (7 Periods)

Comparators: Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open- Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Total Periods: 45

TEXT BOOKS:

1. B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGrawHill Edition2016.
2. Paul. R. Gray & Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.

REFERENCES:

1. T.C. Carusone, D.A. Johns & K. Martin, "Analog Integrated Circuit Design", 2ndEdition, Wiley, 2012.
2. P.E. Allen & D.R.Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
3. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition,Wiley, 2010.

M.Tech. – I Sem

L	T	P	C
3	0	0	3

(EC24DPC102) CMOS DIGITAL IC DESIGN

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- Involve analysis of performance metrics.
- Teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- Teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

COURSE OUTCOMES:

The objective of this course are to:

CO 1: Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,
CO 2: Estimate Delay and Power of Adders circuits.
CO 3: Classify different semiconductor memories.
CO 4: Analyze, design and implement combinational and sequential MOS logiccircuits.
CO 5: Analyze complex engineering problems critically in the domain of digital IC design for conducting research.

UNIT I: (10 Periods)

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output High voltage, Output Low voltage, Gainat gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT II: (10 Periods)

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates andCMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT III: (7 Periods)

Sequential MOS Logic Circuits: Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT IV: (8 Periods)

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT V: (10 Periods)

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Total Periods: 45

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

REFERENCES:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Edition, PHI.

M.Tech. – I Sem

L	T	P	C
3	0	0	3

(EC24DPE101) CAD FOR VLSI

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the fundamentals of VLSI design
- Learn about different levels of design abstraction in VLSI
- Understand the process of physical design
- Gain knowledge in verifying VLSI designs
- Understand how different CAD tools are integrated within a VLSI design flow.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.

CO 2: Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.

CO 3: Practice the application of fundamentals of VLSI technologies

CO 4: Optimize the implemented design for area, timing and power by applying suitable constraints

CO 5: Compare various FPGA hardware ICs.

UNIT I: (7 Periods)

Introduction: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT II: (8 Periods)

Partitioning: Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.

UNIT III: (10 Periods)

Floor Planning: Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint-based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT IV: (10 Periods)

Placement and Routing: Placement–Problem formulation, Classification of placement algorithms, Partitioningbased placement algorithms.

Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT V: (10 Periods)

FPGAs and MCMs: Physical Design Automation of FPGAs and MCMs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

Total Periods: 45

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCES:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, HabibYoussef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley studentEdition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

M.Tech. – I Sem

L	T	P	C
3	0	0	3

(EC24DPE102) HARDWARE FOR DEEP LEARNING

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the Hardware Landscape for Deep Learning
- Explore Hardware Acceleration Techniques
- Evaluate Hardware for Different Deep Learning Applications
- Hands-on Experience with Hardware Deployment
- Understand the Future Trends and Developments in Hardware for DeepLearning
- Understand the Security and Reliability in Hardware for Deep Learning

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand the context of convolutional neural networks and deep learning algorithms.

CO 2: Know how to use convolution in deep learning techniques.

CO 3: Understand the necessity and importance of light weight models with low complexity through specialized hardware architecture

CO 4: Know how to optimize hardware performance in deep neural network applications.

CO 5: Discuss, suggest and evaluate specialized hardware architectures toimplement deep learning algorithms in FPGA and utilize deep learning concepts in resource constrained reliable systems.

UNIT I: (11 Periods)

Introduction to Deep Learning: From AI to DL, Neural Network: Perceptrons, Back Propagation, Over-fitting, Regularization. Deep Networks: Definition, Motivation, Applications, Convolution Neural Network (CNN): Basic architecture, Activation functions, Pooling, Handling vanishing gradient problem, Dropout, Weightinitialization methods, Batch Normalization. Training Neural networks, Additional CNN Components, Famous CNNs, Applications, Software libraries.

UNIT II: (7 Periods)

Computing Convolutions: Mapping Matrix multiplication, Computational Transforms, Accelerator Architectures, Data flow Taxonomy

UNIT III: (7 Periods)

Reducing the Complexity: Light weight models, reducing precision, Aggressive Quantization, pruning & Deep compression.

UNIT IV: (10 Periods)

The Deep Learning Acceleration Landscape: parallelism in deep learning, Traditional programmable hardware, specialized deep learning hardware platforms, deep learning software stack, Specialized research ASICs.

UNIT V: (10 Periods)

FPGAs for Deep Learning: Overview of hardware architectures for deep learning, Effective management of FPGA memory resources, optimizing algorithms and data representation for FPGA arithmetic resources, Integrating hardware and software.

Total Periods: 45

TEXT BOOKS:

1. Ian Goodfellow, Yishuv Bengio and Aaron Courville, "Deep Learning." MIT Press. 2016. ISBN:978-0262035613. Available online for free at: http://www.deeplearningbook.org
2. Vivienne Sze; Yu-Hsin Chen; Tien-Ju Yang; Joel S. Emer, "Efficient Processing of Deep Neural Networks" Morgan & Claypool Publishers, 1stEdition, 2020.
3. Tushar Krishna, Hyoukjun Kwon, Angshuman Parashar, Michael Pellauer, andAnanda

Samajdar, "Data Orchestration in Deep Learning Accelerators", Morgan & Claypool Publishers, 1st Edition, 2020.

REFERENCES:

1. Piotr Antonik, "Application of FPGA to Real-Time Machine Learning",Springer, 2018.
2. Sze, et al. https://eyeriss.mit.edu/ ISCA Tutorial 2019
3. Sze, et al. "Efficient Processing of Deep Neural Networks: A Tutorial and
4. Survey", Proceedings of the IEEE, 2017
5. Prof. Adam Teman https://www.eng.biu.ac.il/temanad/hardware-for-deep-learning/ https://jameswhanlon.com/

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(EC24DPE103) MICROCHIP FABRICATION TECHNIQUES

COURSE OBJECTIVES:

The objective of this course are to:

- Comprehend impact of semiconductor industry on the design of developmentof integrated circuits.
- Acquaint with clean room technology
- Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
- Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and45nm technologies
- Understand packaging principles

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand various stages of fabrication
CO 2: Understand Various packaging techniques and Design rules.
CO 3: Classify various thin films and its characteristics.
CO 4: Formulate fabrication steps to produce functional semiconductor devices, such as transistors, diodes, and integrated circuits.
CO 5: Develop the ability to troubleshoot and solve common problems encountered during microchip fabrication, such as defects, yield issues, and process variations.

UNIT I: (10 Periods)

Introduction to Processing: Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction.

UNIT II: (10 Periods)

Photolithography: Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT III: (7 Periods)

Diffusion and Ion Implantation: Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT IV: (10 Periods)

Film Depositions and Growth: Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT V: (8 Periods)

Yield: Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors. Packaging: Chip characteristics, package functions, package operations

Total Periods: 45

TEXT BOOKS:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. S.M. Sze, VLSI technology, McGraw-Hill Book Company, NY, 1988
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000
4. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000

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(EC24DPE104) ASIC DESIGN

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the fundamentals of Application-Specific Integrated Circuit(ASIC) design
- Learn about different ASIC design methodologies like full-custom, semi-custom, and gate-array approaches
- Study the principles of digital design, including combinational and sequentiallogic, timing analysis, and logic optimization
- Understand the ASIC design flow and Learn about the tools and softwareused at each stage of the design flow
- Understand the challenges and techniques involved in designing mixed-signal ASICs

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand different types of ASICs and their libraries.
CO 2: Understand about programmable ASICs, I/O modules and their interconnects.
CO 3: Gets complete knowledge regarding different methods of software ASICdesign their simulation, testing and construction of ASICs
CO 4: Enhance their problem-solving skills by optimizing ASIC designs for power, performance, and area (PPA), addressing challenges such as power consumption, heat dissipation, and clock distribution
CO 5: Gain experience in collaborating on ASIC design projects, developing project management skills, and understanding the importance of teamwork in large-scale design efforts.

UNIT I: (8 Periods)

Introduction to ASICs: Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT II: (7 Periods)

Programmable ASICs and Programmable ASIC Logic Cells: The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues,Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT III: (10 Periods)

I/O Cells and Interconnects & Programmable ASIC Design Software: DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT IV: (10 Periods)

Low Level Design Entry and Logic Synthesis: Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the Viterbi decoder.

UNIT V: (10 Periods)

Simulation, Test and ASIC Construction: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern

Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

Total Periods: 45

TEXT BOOKS:

1. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.
2. L.J.Herbst, "Integrated Circuit Engineering", Oxford Science Publications, 1996.

REFERENCES:

1. Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis using Synopsis Design Compiler", 2nd Edition, Kluwer Academic, 2001.

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(EC24DPE105) CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

COURSE OBJECTIVES:
The objective of this course are to:
- Understand the basic concepts and differences between Complex Programmable Logic Devices (CPLDs) and Field-Programmable Gate Arrays(FPGAs)
- Understand the process of synthesis in CPLDs and FPGAs
- Learn the methods for design entry in CPLDs and FPGAs and differentconfiguration modes
- Understand the steps involved in implementing a design on CPLDs and FPGAs
- Understand the methods for testing and debugging CPLD and FPGA designs

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
- **CO 1:** Acquire knowledge about various architectures and device technologies of PLD's.
- **CO 2:** Comprehend FPGA Architectures.
- **CO 3:** Analyze System level Design and their application for Combinational and Sequential Circuits.
- **CO 4:** Get familiar with Anti-Fuse Programmed FPGAs.
- **CO 5:** Apply knowledge of this subject for various design applications.

UNIT I: (10 Periods)
Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices– Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT II: (10 Periods)
Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT III: (8 Periods)
SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT IV: (7 Periods)
Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT V: (10 Periods)
Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Total Periods: 45

TEXT BOOKS:
1. Field Programmable Gate Array Technology – Stephen M. Trimberger, Springer international Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, CengageLearning.

REFERENCES:
1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad,

Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier,Newnes.
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern SemiconductorDesign Series.

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(EC24DPE106) ORGANIC ELECTRONICS

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the basic principles and scope of organic electronics
- Learn about the chemical structure, properties, and synthesis of organic semiconductors
- Understand the operating principles of various organic electronic devices
- Explore different types of organic materials used in electronics
- Explore the current and emerging applications of organic electronics

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand "what is organic electronics good for?"
CO 2: Learn about structure and properties of organic materials and devices, their functioning and properties, and field of applications
CO 3: Explain charge transport, energy levels and doping in organic electronic materials
CO 4: Exemplify the optical properties and applications of organic electronicmaterials, such as in displays and photovoltaic systems
CO 5: Exemplify the architecture, characterization, and utilization of electronic components based on organic electronic materials (such as transistors)

UNIT I: (7 Periods)

Introduction to Organic electronics: Overview, history, Common language, crystal structure & binding.

UNIT II: (10 Periods)

Optical properties of organic semiconductors: Born-Oppenheimer approximation & Franck-Condon principle; Transitions between states: Fermi's golden rule; Excitons, Spin, Energy transfer; Exciton diffusion and recombination.

UNIT III: (8 Periods)

Electronic properties of organic semiconductors: Energy bands, electron transport, conduction, mobility, doping, HJs.

UNIT IV: (10 Periods)

Materials growth & purification, device patterning, packaging Light Emitters: basics, efficiency, fluorescence, phosphorescence, TADF, Rolloff, White OLEDs, outcoupling, reliability.

UNIT V: (10 Periods)

Light Detectors: basics, efficiency, architect, materials, transparency, Multijunction OPV, reliability, modules.

Transistors: basics, architectures, morphology, reliability, organic transistor circuit applications.

Total Periods: 45

TEXT BOOKS:

1. Organic Electronics: Foundations to Applications, Stephen R. Forrest, Oxford University Press, 2020, 1st edition.

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(EC24DRM101) RESEARCH METHODOLOGY AND IPR

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the purpose and significance of research in academic andprofessional contexts
- Understand the components of a research proposal
- Understand the importance of selecting appropriate tools and techniques fordata collection.
- Understand the process of publishing research in academic journals
- Understand the concept and importance of intellectual property (IP) inresearch and innovation.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand research problem formulation.

CO 2: Analyze research related information and Follow research ethics

CO 3: Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.

CO 4: Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasise the need of information about Intellectual Property Right to be promoted among students in general &engineering in particular.

CO 5: Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth & social benefits.

UNIT I: (6 Periods)

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation and Necessary instrumentations.

UNIT II: (6 Periods)

Effective literature study approaches, analysis Plagiarism, and Research ethics. Effective technical writing, how to write report, Paper Developing a ResearchProposal, Format of research proposal, a presentation and assessment by a review committee

UNIT III: (6 Periods)

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT IV: (6 Periods)

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT V: (6 Periods)

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Total Periods: 30

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.

REFERENCES:

1. Mayall , "Industrial Design", McGraw Hill, 1992.
2. Niebel , "Product Design", McGraw Hill, 1974.
3. Asimov , "Introduction to Design", Prentice Hall, 1962.
4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property inNew Technological Age", 2016.
5. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

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(EC24DPC103) CMOS ANALOG IC DESIGN LAB

COURSE OBJECTIVES:

The objective of this course are to:

- Design and implement any TEN Experiments using CMOS 130nm Technology with Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent standard software.
- Implement LAYOUTS of any SIX Experiments usingCMOS 130nm Technology with Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software, and Compare the results withPre-Layout Simulation.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Explain the VLSI Design Methodologies using VLSI design tool.
CO 2: Grasp the significance of various CMOS analog circuits in full-custom ICDesign flow
CO 3: Explain the Physical Verification in Layout Design
CO 4: Fully appreciate the design and analyze of analog and mixed signal simulation
CO 5: Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

List of Experiments

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:

Software:

Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator

Hardware:

Personal Computer with necessary peripherals, configuration and operating system.

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(EC24DPC104) CMOS DIGITAL IC DESIGN LAB

COURSE OBJECTIVES:

The objective of this course are to:

- Design and implement the Circuit and Layoutof any TEN Experiments using CMOS 130nm Technology with Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Explain the VLSI Design Methodologies using any VLSI design tool.
CO 2: Grasp the significance of various design logic Circuits in full-custom ICDesign.
CO 3: Explain the Physical Verification in Layout Extraction.
CO 4: Fully appreciate the design and analyze of CMOS Digital Circuits.
CO 5: Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

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(EC24DMC101) ENTREPRENEURSHIP AND INCUBATION

COURSE OBJECTIVES:
The objective of this course are to:
- Make the student understand about Entrepreneurship
- Enable the student in knowing various sources of generating new ideas insetting up of New enterprise
- Facilitate the student in knowing various sources of finance in starting upof a business
- Impart knowledge about various government sources which providefinancial assistance to entrepreneurs/ women entrepreneurs
- Encourage the student in creating and designing business plans

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
- **CO 1:** Understand the concept of Entrepreneurship and challenges in the world of competition.
- **CO 2:** Apply the Knowledge in generating ideas for New Ventures.
- **CO 3:** Analyze various sources of finance and subsidies to entrepreneur/women Entrepreneurs.
- **CO 4:** Evaluate the role of central government and state government in promoting Entrepreneurship.
- **CO 5:** Create and design business plan structure through incubations.

UNIT I: **(6 Periods)**
Entrepreneurship - Concept, knowledge and skills requirement - Characteristics of successful entrepreneurs - Entrepreneurship process - Factors impacting emergence of entrepreneurship - Differences between Entrepreneur and Intrapreneur - Understanding individual entrepreneurial mindset and personality - Recent trends in Entrepreneurship.

UNIT II: **(6 Periods)**
Starting the New Venture - Generating business idea – Sources of new ideas & methods of generating ideas - Opportunity recognition - Feasibility study - Market feasibility, technical/ operational feasibility - Financial feasibility - Drawing business plan – Preparing project report - Presenting business plan to investors.

UNIT III: **(6 Periods)**
Sources of finance - Various sources of Finance available - Long term sources - Short term sources - Institutional Finance – Commercial Banks, SFC's in India - NBFC's in India - their way of financing in India for small and medium business - Entrepreneurship development programs in India - The entrepreneurial journey- Institutions in aid of entrepreneurship development.

UNIT IV: **(6 Periods)**
Women Entrepreneurship - Entrepreneurship Development and Government - Roleof Central Government and State Government in promoting women Entrepreneurship - Introduction to various incentives, subsidies and grants– Export - oriented Units - Fiscal and Tax concessions available - Women entrepreneurship - Role and importance - Growth of women entrepreneurship in India - Issues and Challenges - Entrepreneurial motivations.

UNIT V: **(6 Periods)**
Fundamentals of Business Incubation - Principles and good practices of business incubation- Process of business incubation and the business incubator and how theyoperate and influence the Type/benefits of incubators - Corporate/educational / institutional incubators – Broader business incubation environment - Pre-Incubationand Post - Incubation process - Idea lab, Business plan structure - Value proposition

Total Periods: 30

TEXT BOOKS:

1. D F Kuratko and T V Rao, "Entrepreneurship" - A South-Asian Perspective – Cengage Learning, 2012. (For PPT, Case Solutions Faculty may visit: login.cengage.com)
2. Nandan H, "Fundamentals of Entrepreneurship", PHI, 2013

REFERENCES:

1. Vasant Desai, "Small Scale Industries and Entrepreneurship", Himalaya Publishing 2012.
2. Rajeev Roy "Entrepreneurship", 2nd Edition, Oxford, 2012.
3. Stuart Read, Effectual "Entrepreneurship", Routledge, 2013.

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(EC24DPC201) CMOS MIXED SIGNAL DESIGN

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the fundamentals of mixed-signal design
- Learn about the applications and significance of mixed-signal circuits in modern electronics
- Study the basic building blocks of CMOS circuits
- Understand the various architectures of ADCs and DACs
- Study the design and optimization of digital circuits for speed, area, andpower efficiency

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Demonstrate first order filter with least interference

CO 2: Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.

CO 3: Design different A/D, D/A, modulators, demodulators and different filter forreal time applications

CO 4: Develop the ability to optimize mixed-signal circuits for power efficiency and performance, applying low-power design techniques and understanding trade-offs between speed, area, and power consumption

CO 5: Explore advanced applications of CMOS mixed-signal design in areas such as wireless communication, sensor interfaces, data converters, and signal processing.

UNIT I: (8 Periods)

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

UNIT II: (10 Periods)

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT III: (10 Periods)

Data Converter: Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT IV: (10 Periods)

A to D Converters: Nyquist Rate A/D Converters Successive approximation converters, Flash converter,Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time- interleaved converters.

UNIT V: (7 Periods)

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher ordermodulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A

Total Periods: 45

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

REFERENCES:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- RudyVan De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009

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(EC24DPC202) PHYSICAL DESIGN AUTOMATION

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the role and importance of physical design automation in the ICdesign
- Understand the role of design rules and technology files in guiding thephysical design
- Learn the principles of partitioning and floor planning in VLSI design
- Study the process of physical verification
- Learn about simulation and synthesis techniques

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand relation between automation algorithms and constraints posed byVLSI technology.
CO 2: Adopt algorithms to meet critical design parameters.
CO 3: Design area efficient logics by employing different routing algorithms andshape functions.
CO 4: Simulate and synthesis different combinational and sequential logics
CO 5: Acquire the ability to optimize physical designs for key metrics such as performance, power, and area (PPA), balancing trade-offs to meet design specifications.

UNIT I: (8 Periods)

VLSI Design Automation Tools: Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT II: (10 Periods)

Layout: Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT III: (7 Periods)

Floor planning and routing: Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT IV: (10 Periods)

Simulation and Logic Synthesis: Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis.

UNIT V: (10 Periods)

High-Level Synthesis: Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspectsof assignment, High level transformations.

Total Periods: 45

TEXT BOOKS:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998.
2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer,1999.

REFERENCES:

1. S.M. Sait,H.Youssef, VLSI Physical Design Automation, World scientific, 1999.
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

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(EC24DPE201) MEMS SYSTEM DESIGN

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the fundamentals of Microelectromechanical Systems (MEMS)and their applications across various industries
- Study the materials commonly used in MEMS
- Learn about MEMS fabrication process techniques
- Explore the various sensing mechanisms used in MEMS devices
- Learn about the design and operation of MEMS sensors for measuringphysical parameters

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

- **CO 1:** Understand the basic concepts of MEMS technology and working of MEMS devices.
- **CO 2:** Understand and select different materials for current MEMS devices andcompeting technologies for future applications.
- **CO 3:** Understanding the concepts of fabrication process of MEMS, Design andPackaging Methodology.
- **CO 4:** Analyze the various fabrication techniques in the manufacturing of MEMS Devices
- **CO 5:** Gain expertise in testing and characterizing MEMS devices, including techniques for measuring mechanical properties, electrical performance, and environmental sensitivity.

UNIT I: (7 Periods)

Introduction to MEMS: Introduction to MEMS & Real world Sensor/Actuator examples (DMD, Air-bag,pressure sensors).MEMS Sensors in Internet of Things (IoT), Bio-MedicalApplications

UNIT II: (10 Periods)

MEMS Materials and Their Properties: Materials (eg. Si, SiO2, SiN, Cr, Au, Ti, SU8, PMMA, Pt); Important properties: Young modulus, Poisson's ratio, density, piezo-resistive coefficients, TCR, Thermal Conductivity, Material Structure. Understanding Selection of materials based on applications.

UNIT III: (8 Periods)

MEMS Fab Processes – 1: Understanding MEMS Processes & Process parameters for: Cleaning, Growth &Deposition, Ion Implantation & Diffusion, Annealing, Lithography. Understanding selection of Fab processes based on Applications.

UNIT IV: (10 Periods)

MEMS Fab Processes – 2: Understanding MEMS Processes & Process parameters for: Wet & Dry etching, Bulk& Surface Micromachining, Die, Wire& Wafer Bonding, Dicing, Packaging. Understanding selection of Fab processes based on Applications.

UNIT V: (10 Periods)

MEMS Devices: Architecture, working and basic quantitative behaviour of Cantilevers, Micro heaters, Accelerometers, Pressure Sensors, Micro mirrors in DMD, Inkjet printer-head. Understanding steps involved in Fabricating above devices.

Total Periods: 45

TEXT BOOKS:

1. An Introduction to Micro electromechanical Systems Engineering; 2nd Editionby N.Maluf, K Williams; Publisher: Artech House Inc
2. Practical MEMS - by Ville Kaajakari; Publisher: Small Gear Publishing
3. Micro system Design - by S. Senturia; Publisher: Springer

REFERENCES:

1. Analysis and Design Principles of MEMS Devices –Minhang Bao; Publisher:Elsevier Science.
2. Fundamentals of Micro fabrication - by M. Madou; Publisher:CRC Press;2nd edition
3. Micro Electro Mechanical System Design - by J. Allen; Publisher: CRC Press
4. Micro machined Transducers Sourcebook - by G. Kovacs; Publisher: McGraw-Hill

M.Tech. – II Sem.

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(EC24DPE202) SEMICONDUCTOR MEMORY DESIGN AND TESTING

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the fundamental concepts of semiconductor memories
- Study the architecture and operations of SRAM, DRAM
- Understand the characteristics and design of non-volatile memories,including ROM, PROM, EPROM, EEPROM, and Flash memory
- Understand the design of fault-tolerant memory systems and techniques forenhancing memory reliability
- Study the implementation and effectiveness of Advanced Memory and High-density Memory Packing Technologies

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories.

CO 2: Build fault models for memory testing.

CO 3: Analyze different parameters that lead malfunctioning of memories.

CO 4: Design reliable memories with efficient architecture to improve processestimes and power

CO 5: Develop skills in designing semiconductor memories with testability in mind, including integrating test structures and developing effective test strategies for memory devices.

UNIT I: (10 Periods)

Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT II: (10 Periods)

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT III: (7 Periods)

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT IV: (10 Periods)

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT V: (8 Periods)

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memorycards, High Density Memory Packaging Future Directions.

Total Periods: 45

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma-2002, Wiley.

REFERENCES:

1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu,First Edition. Prentice all.

M.Tech. – II Sem.

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(EC24DPE203) VLSI TEST AND TESTABILITY

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the importance of testing in the VLSI design
- Study common fault models used in VLSI testing
- Learn about techniques for generating test patterns
- Study the automatic test pattern generation (ATPG) and fault simulation algorithms
- Learn about key DFT techniques such as scan design, boundary scan, andbuilt-in self-test (BIST)

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Identify the significance of testable design
CO 2: Understand the concept of yield and identify the parameters influencing the same.
CO 3: Specify fabrication defects, errors and faults
CO 4: Implement combinational and sequential circuit test generation algorithms
CO 5: Identify techniques to improve fault coverage.

UNIT I: (10 Periods)

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault, error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits.

UNIT II: (7 Periods)

Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms.

UNIT III: (10 Periods)

Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods. Difference between combinational and sequential circuittesting, five and eight valued algebra, and Scan chain-based testing method.

UNIT IV: (10 Periods)

D-algorithm procedure, Problems, PODEM Algorithm. Problems on PODEM Algorithm. FAN Algorithm. Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan-based design.

UNIT V: (8 Periods)

Classical scan-based design, System level DFT approaches Test pattern generation for BIST, Circular BIST. BIST Architectures. Testable memory design-Test Algorithms-Test generation for Embedded RAMs

Total Periods: 45

TEXT BOOKS:

1. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990.

REFERENCES:

1. Stroud, "A Designer's Guide to Built-in Self-Test", Kluwer Academic Publishers, 2002.
2. M. Bushnell and V. Agrawal, "Essentials of Electronic Testing for Digital,Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.
3. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989.

M.Tech. – II Sem.

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(EC24DPE204) BIO-MEDICAL CMOS ICs

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the role and significance of CMOS technology in the developmentof bio-medical ICs
- Study the Electrode Design concepts and Standards
- Explore techniques for optimizing the performance of analog circuits in bio-medical ICs
- Study the application of digital signal processing (DSP) techniques to bio-medical data
- Explore the design considerations for bio-medical wireless and Short distance Wireless Communications

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Familiarize the concepts of used to design biomedical ICs
CO 2: Acquire knowledge to design various electrodes
CO 3: Learn the design of various biomedical amplifiers
CO 4: Analyze and implement various low power ADCs for biomedical applications
CO 5: Acquire knowledge about types of short-range wireless communication

UNIT I: (10 Periods)

Introduction to Bio-Medical CMOS ICs: Introduction to Bioelectricity, Electrical Properties of the Human body, Equivalent Circuit Model of Tissues and Organs, Biomedical Devices, Current Research Trends in Biomedical Electrical Instruments.

UNIT II: (8 Periods)

Electrode Design, Modern Disposable Electrodes, Solid Conductive Adhesive Electrodes, Implant Electrodes, Microelectrodes, Electrode Standards.

UNIT III: (10 Periods)

Readout Circuits: Biopotential Acquisition, Power Efficient Instrumentation Amplifier Topologies for Biopotential Signal Extraction, Current Mode Instrumentation Amplifiers, Examples of ICs for Biopotential Acquisition.

UNIT IV: (10 Periods)

Basic operation principles and architectures as well as the most recent research results of low power CMOS ICs. Low power ADCs for Bio-Medical Applications, Low Power Bio-Medical DSP.

UNIT V: (7 Periods)

Bio-Medical Wireless Communication, Introduction to Short distance Wireless Communications.

Total Periods: 45

TEXT BOOKS:

1. Hoi-Jun Yoo: Chris van Hoof, "Integrated Circuits and Systems- Bio Medical CMOS ICs", Springer, 2010.
2. D C Reddy "Biomedical Signal Processing: Principles and Techniques", Tata McGraw-Hill Publishing Co. Ltd, 2005.

REFERENCES:

1. R M Rangayyan, "Biomedical Signal Analysis: A case Based Approach", IEEE Press, John Wiley and Sons. Inc., 2002.
2. Jacob Fraden, "Handbook of Modern Sensors: Physics, Designs, and Applications", Springer, 2010
3. J. G. Webster, "The Measurement, Instrumentation and Sensors Handbook vol. 1", CRC Press, 1st Edition, 1998.

M.Tech. – II Sem.

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(EC24DPE205) ELECTRONIC PACKAGING AND 3D IC TECHNOLOGIES

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the role of electronic packaging and Learn about the evolution of packaging technologies
- Study the role of through-silicon vias (TSVs) in 3D ICs and Learn about thedesign and fabrication of TSVs
- Understand the concept of 3D technology and Packaging techniques
- Understand the thermal and mechanical challenges unique to 3D ICs
- Explore the applications and trends in 3D ICs

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand the role of packaging in the computer, telecommunication,automotive, medical and consumer electronics industry

CO 2: Learn the fundamentals of electrical packaging design, design for reliability, thermal management

CO 3: Analyze the performance of various TSVs for 3-D ICs

CO 4: Identify the packaging materials with their appropriate properties

CO 5: Analyze the thermal issues in electronic packaging and 3D ICs.

UNIT I: (10 Periods)

Functions of an Electronic Package, Packaging Hierarchy, Driving Forces on Packaging Technology. Materials for Microelectronic packaging, Packaging materialsproperties, ceramics, polymers and metals in packaging. Electrical Anatomy of systems packaging, signal distribution, power distribution, electromagnetic interference.

UNIT II: (10 Periods)

Through Silicon Via: Materials, properties of TSVs, fabrication of TSVs, challengesfor TSV implementation. Modeling and performance analysis of Copper-based, CNT-based, GNR-based TSVs. Liners in TSVs.

UNIT III: (10 Periods)

3D-Technology and Packaging Techniques: Silicon interposer technology, Through Silicon Vias (TSVs). Hybrid packaging technique, Silicon-Less Interconnect technology. 3D Integrated Architectures

UNIT IV: (7 Periods)

Physical Design and Thermal Management Techniques for 3-D ICs

UNIT V: (8 Periods)

Case Study: clock distribution networks for 3-D ICs, Trends in Packaging.

Total Periods: 45

TEXT BOOKS:

1. Vasilis F Pavlidis, E G Friedman, Three-Dimensional Integrated Circuit Design, Morgan Kaufmann Publishers, Elsevier, 2009.
2. Rao R. Tummala, Fundamentals of Microsystem Packaging, McGraw Hill, 2001.

REFERENCES:

1. John H. Lau, Through-Silicon Vias for 3D Integration, McGraw Hill, 2012.
2. Related research papers.

Other Suggested Readings:

1. NPTEL Courses (https://onlinecourses.nptel.ac.in/noc23_cs07/preview)

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(EC24DPE206) VLSI SIGNAL PROCESSING

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the fundamentals of VLSI and its role in implementing signalprocessing
- Learn about common DSP algorithms and implementation of these algorithms in VLSI
- Understand the concepts of Systolic Architecture Design in VLSI signalprocessing
- Learn about the VLSI-based signal processing applications in Fast convolution algorithms
- Study the Low Power Design issues in VLSI signal processing

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Modify the existing or new DSP architectures suitable for VLSI.
CO 2: Understand the concepts of folding and unfolding algorithms and applications.
CO 3: Implement fast convolution algorithms
CO 4: Understand the trade-offs involved in different architectural choices and their impact on performance and power consumption
CO 5: Develop skills in designing and analyzing digital filters for VLSI implementation, including FIR and IIR filters.

UNIT I: (10 Periods)

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT II: (10 Periods)

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT III: (8 Periods)

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selectionof Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT IV: (7 Periods)

Fast Convolution: Introduction – Cook - Toom Algorithm – Winogard algorithm – Iterated Convolution –Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT V: (10 Periods)

Low Power Design: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Total Periods: 45

TEXT BOOKS:

1. Keshab K. Parthi, VLSI Digital signal processing systems, design and implementation, Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and informationprocessing, McGraw Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing,Prentice Hall, 1985.

M.Tech. II Sem.

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(EC24DPC203) MIXED SIGNAL IC DESIGN LAB

COURSE OBJECTIVES:
The objective of this course are to:
- Understand Mixed-Signal Concepts
- Design and Simulation Skills
- Practical Implementation
- Circuit Analysis and Debugging

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
- **CO 1:** Gain a solid understanding of the fundamental concepts in mixed-signal design, including the integration of analog and digital circuits
- **CO 2:** Develop hands-on experience with industry-standard electronic design automation (EDA) tools used for mixed-signal IC design, such as Cadence, Mentor Graphics, or Synopsys.
- **CO 3:** Learn to simulate, verify, and optimize mixed-signal circuits using Cadence, Mentor Graphics, or Synopsys.
- **CO 4:** Design and implement digital blocks, including logic gates, flip-flops, and counters, within a mixed-signal environment
- **CO 5:** Develop skills in verifying and testing mixed-signal circuits, including performing simulations, running test benches, and analyzing results.

Cycle 1:
1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   a. Two stage cross coupled clamped comparator
   b. Strobed Flip-flop
3) Data converter

Cycle 2:
1) Switched capacitor circuits
   a. Parasitic sensitive integrator
   b. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Band gap reference circuit
5) Layouts of All the circuits Designed and Simulated

Software:
Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

Hardware:
Personal Computer with necessary peripherals, configuration and operating system.

TEXT BOOKS:
1) David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2) R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley,1986.
3) Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley,1999.
4) Alan Hastlings, The art of Analog Layout, Wiley, 2005.

M.Tech. II Sem.

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(EC24DPC204) PHYSICAL DESIGN AUTOMATION LAB

COURSE OBJECTIVES:

The objectives of the Course are

- Understand Physical Design Flow
- Hands-On Tool Experience
- Timing Analysis and Optimization
- Power Analysis and Optimization
- Understand Design for Testability (DFT)

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Gain a comprehensive understanding of the key concepts in physical design automation, including floor-planning, placement, routing, and timing analysis.

CO 2: Understand the physical design flow, including the steps involved from initial design specifications to final tape-out.

CO 3: Apply industry-standard methodologies for physical design, including integration with digital and analog design elements.

CO 4: Gain skills in creating efficient floorplans for ICs, optimizing the placement of cells and blocks to meet design constraints such as area, power, and performance.

CO 5: Develop skills in performing static timing analysis to ensure that the design meets its performance requirements.

Cycle 1:

1) Graph algorithms
    a) Graph search algorithms
        i. Depth first search
        ii. Breadth first search
    b) Spanning tree algorithm
        i. Kruskal"s algorithm
    c) Shortest path algorithm
        i. Dijkstra algorithm
        ii. Floyd- Warshall algorithm
    d) Steiner tree algorithm
2) Computational geometry algorithm
    a) Line sweep method
    b) Extended line sweep method

Cycle 2:

3) Partitioning algorithms
    a) Group migration algorithms
        i. Kernighan –Lin algorithm
        ii. Extensions of Kernighan-Lin algorithm
            i) Fiduccias –Mattheyses algorithm
            ii) Goldberg and Burstein algorithm
    b) Simulated annealing and evolution algorithms
        i. Simulated annealing algorithm
        ii. Simulated evolution algorithm
            iii) Metric allocation method
4) Floor planning algorithms
        i. Constraint based methods
        ii. Integer programming based methods
        iii. Rectangular dualization based methods
        iv. Hierarchical tree based methods
        v. Simulated evolution algorithms
        vi. Time driven Floor planning algorithms

5) Routing algorithms
    a) Two terminal algorithms
        i. Maze routing algorithms
            i) Lee"s algorithm
            ii) Soukup"s algorithm
            iii) Hadlock algorithm
    b) Line-Probe algorithm
    c) Shortest path based algorithm
        i. Multi terminal algorithm
    d) Stenier tree based algorithm
        i. SMST algorithm
        ii. Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

TEXT BOOKS:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition,Kluwer Academic,1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook ofAlgorithms for Physical Design Automation, CRC Press,2008.

M.Tech. II Sem.

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(EG24DAC201) ENGLISH FOR RESEARCH PAPER WRITING

COURSE OBJECTIVES:

The objective of this course are to:

- Conceptualize various components of academic writing.
- Enhance and use academic vocabulary.
- Plan and write quality research papers in their respective field.
- Ensure the good quality of paper at very first-time submission

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Become aware of various components of academic writing
CO 2: Improve and use academic vocabulary while writing a research Papers
CO 3: Plan and write quality research papers in their respective field
CO 4: Develop a strong command of academic language, including technical vocabulary, complex sentence structures, and appropriate tone
CO 5: Learn proper citation practices, including the use of different citation styles (e.g., APA, MLA, IEEE) and the importance of avoiding plagiarism.

UNIT I: **(6 Periods)**

Scientific Writing: What is scientific writing – Language in scientific writing – Use and misuse of English –Elements of scientific writing - Paraphrasing and Plagiarism - Hedging and Criticizing – How to identify research problem

UNIT II: **(6 Periods)**

Writing Title and Abstract: Strategies for writing effective title – Planning and preparing your abstract - Things to consider while writing abstract – Useful phrases for writing abstract.

UNIT III: **(6 Periods)**

Organizing Review of the Literature; Methods of Data Collection andData Analysis: What is review of the literature - Techniques of reading and citing various studies relevant to the study – Things to consider while organizing review of the literature –useful phrases while writing review of the literature - Introduction to variousmethods of data collection – Preparing tools and describing them - How to interpret and analyze data.

UNIT IV: **(6 Periods)**

Writing Findings, Discussion and Conclusion: Useful vocabulary while writing findings, discussion, and conclusion – elaboration ofthe findings - Preparing and describing charts and graphs – how to organize.

UNIT V: **(6 Periods)**

Preparing References, Appendixes and Proof reading The Paper: Various styles of referencing and bibliography (APA, MLA, Oxford, Harvard, Chicago) –Organizing and preparing Appendixes – Various strategies of proofreading.

Total Periods: 30

TEXT BOOKS:

1. Adrian Wallwork, (2011). English for Writing Research Papers. SpringerNew York
2. Goldbort R (2006) Writing for Science, Yale University Press (available onGoogle Books)

REFERENCES:

1. Kate L. Turabian, "A Manual for Writers of Research Papers, Theses, and Dissertations, Seventh Edition: Chicago Style for Students and Researchers [7th ed.] Chicago, Guides to Writing, Editing, and Publishing, 2007.

M.Tech. – III Sem.

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(EC24DPE301) BI-CMOS TECHNOLOGY AND APPLICATIONS

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the fundamentals of Bi-CMOS technology
- Study about design Considerations for MOSFET's and Bi-CMOS Device Scaling
- Study the structure and operation of Bi-CMOS devices
- Understand the design properties of Bi-CMOS Digital Integrated Circuits
- Learn about the use of Bi-CMOS technology in high-speed digital circuits

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Demonstrate in-depth knowledge in Bi-CMOS Technology.
CO 2: Analyze complex engineering problems critically for conducting research in Bi-CMOS Technology.
CO 3: Solve engineering problems with wide range of solutions in Radio frequency Integrated circuits.
CO 4: Realize different digital circuits using Bi-CMOS Technology
CO 5: Develop techniques for optimizing the performance and power consumption of Bi-CMOS circuits.

UNIT I: (8 Periods)

Bi-CMOS Process Technology: CMOS Process Technology, Bipolar Process Technology, Isolation in CMOS andBipolar Technologies, Bi-CMOS Technology, Bi-CMOS Design Rules.

UNIT II: (10 Periods)

Device Design Considerations: Design Considerations for MOSFET's, Design Considerations for Bipolar Transistors,Bi-CMOS Device Design Considerations.
Bi-CMOS Device Scaling: MOS Device Scaling, Bipolar Device Scaling.

UNIT III: (10 Periods)

Modeling of the MOS Transistor: MOSFET Structure and Operation, SPICEModels of the MOS Transistor, Analytical Model for Short-Channel MOS Devices.
Modeling of the Bipolar Transistor: BJT Structure and Operation, Ebers-MollModel, Bipolar Models in SPICE.

UNIT IV: (10 Periods)

Bi-CMOS Digital Integrated Circuits: BiMOS Totem-Pole Inverter: DC Characteristics, Transient Analysis, Delay Dependence on the Device Parameters, Bi-CMOS Circuit Design, Comparing CMOS and Bi-CMOS Inverters Speed, Bi-CMOS Gates.

UNIT V: (7 Periods)

Bi-CMOS Digital Circuit Applications: Adders, Multiplier, Random Access Memory, Programmable Logic Arrays, Bi-CMOSLogic Cells, Bi-CMOS Gate Arrays.

Total Periods: 45

TEXT BOOKS:

1. Sherif H.K. Embabi, AbdellatifBellaouar& Mohamed I. Elmasry "Digital Bi-CMOS Integrated Circuit Design" Springer Science+ BusÎness Media, LLC.
2. A L ALVAREZ, BICMOS Technology & Applications, Kluwer Academic Publishers.

REFERENCES:

1. Kiat-Seng yeo, Samir S. Rofail, Wang-Ling Goh, CMOS/Bi-CMOS ULSI,Pearson Education.
2. James C. Daly, Denis P. Galipeau, Analog Bi-CMOS Design: Practices &Pitfalls, CRC Press
3. KlaasJan de Langen, Johan Huijsing, Compact Low-Voltage and High-SpeedCMOS, Bi-CMOS and Bipolar Operational Amplifiers, Springer Science

M.Tech. – III Sem.

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(EC24DPE302) OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the role of optimization in VLSI Design and its importance in improving circuit performance
- Study how to formulate optimization problems in VLSI design
- Understand the techniques for Convex Optimization in VLSI circuits
- Study the concepts of Genetic Algorithm
- Learn the GA Routing Procedures and Power Estimation techniques

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand basics of statistical modeling
CO 2: Analyze performance of CMOS circuits with respect to power, area and speed
CO 3: Gets complete knowledge regarding the various algorithms used foroptimization of power and area.
CO 4: Gain a comprehensive understanding of optimization principles and techniques relevant to VLSI design
CO 5: Develop skills in optimizing layout and physical design, including placement and routing of VLSI circuits.

UNIT I: (10 Periods)

Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT II: (10 Periods)

Statistical Performance, Power and Yield Analysis: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT III: (8 Periods)

Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Polynomial fitting.

UNIT IV: (10 Periods)

Genetic Algorithm: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, mapping for FPGA-Automatic test generation-Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement GASP algorithm- unified algorithm.

UNIT V: (7 Periods)

GA Routing Procedures and Power Estimation: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA Standard cell placement – GA for ATG-problem encoding-fitness function-GA Vs Conventional algorithm.

Total Periods: 45

TEXT BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power –Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation –Pinaki Mazumder, E. Mrudnick, Prentice Hall, 1998.

REFERENCES:

1. Convex Optimization- Stephen Boyd, Lieven Vandenberghe, Cambridge University Press,2004

M.Tech. – III Sem.

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(EC24DPE303) SYSTEM ON CHIP ARCHITECTURE

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the concept of System on Chip (SoC) Architecture and its role in integrating multiple system components into a single chip
- Study the integration of various processor types in SoCs
- Explore memory architectures used in SoCs
- Study the interconnect architectures and communication networks used inSoCs
- Study real-world applications of SoCs in various industries and Analyse casestudies of successful SoC designs

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Get complete basics related to SoC architecture and different approachesrelated to SoC Design.
CO 2: Able to select an appropriated robust processor for SoC Design
CO 3: Able to Select an appropriate memory for SoC Design.
CO 4: Realize real time case studies
CO 5: Develop skills in verifying and testing SoCs to ensure functionality, performance, and reliability.

UNIT I: (8 Periods)

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approachfor SOC Design, System Architecture and Complexity.

UNIT II: (10 Periods)

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements inInstruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT III: (10 Periods)

Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT IV: (10 Periods)

Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V: (7 Periods)

Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

Total Periods: 45

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk,Wiely India Pvt. Ltd.

2. ARM System on Chip Architecture – Steve Furber, 2nd Edition, 2000, AddisonWesley Professional.

REFERENCES:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques – PrakashRashinkar, PeterPaterson and Leena Singh L, 2001, Kluwer Academic Publishers

M.Tech. – III Sem.

L	T	P	C
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(EC24DOE301) EMBEDDED SYSTEM DESIGN

COURSE OBJECTIVES:

The objective of this course are to:

- Understand the technologies and techniques underlying in developing anembedded system
- Study the architecture of embedded systems and learn about the Cypress Programmable System on Chip (PSoC)
- Understand the concept of Embedded System product Development Life cycle(EDLC)
- Explore the Features of an Operating System
- Understand the basic concepts of Embedded System DevelopmentEnvironment and Hardware testing methods like ICT

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Explore various general purpose embedded system applications
CO 2: Appreciate the methods adapted for the development of a typical embedded system.
CO 3: Get introduced to RTOS and related mechanisms.
CO 4: Build embedded systems for real-time applications
CO 5: Debug digital embedded systems and solve complex problems.

UNIT I: **(10 Periods)**

Introduction to Embedded system, embedded system examples, Parts of EmbeddedSystem Typical Processor architecture, Power supply, clock, Cache memory, memory interface, interrupt, I/O ports, Buffers, Programmable Devices, ASIC etc. Bus architecture -I2C, SPI, AMBA, CAN. Memory Technologies – EPROM, Flash,OTP, SRAM, DRAM, SDRAM etc.

UNIT II: **(7 Periods)**

Introduction to Cypress Programmable System on Chip (PSoC). Structure of PSoC, PSoC Designer, PSoC Modules, Interconnects, Memory Management, Global Resources, Design Examples

UNIT III: **(10 Periods)**

Embedded System product Development Life cycle (EDLC), Specifications, Component selection, Schematic Design, PCB layout, fabrication and assembly. Product enclosure Design and Development. Concept of firmware, operating systemand application programs. Power supply Design. External Interfaces.

UNIT IV: **(10 Periods)**

Basic Features of an Operating System, Kernel Features [polled loop system,interrupt driven system, multi rate system], Processes and Threads, Context Switching, Scheduling [RMA, EDF, fault tolerant scheduling], Inter-process Communication, real Time memory management [process stack management, dynamic allocation], I/O [synchronous and asynchronous I/O, Interrupts Handling, Device drivers], RTOS [VxWorks, RT-LINUX].

UNIT V: **(8 Periods)**

Embedded System Development Environment – IDE, Cross compilation, Simulators/Emulators, Hardware Debugging. Hardware testing methods like Boundary Scan, In Circuit Testing (ICT) etc.

Total Periods: 45

TEXT BOOKS:

1. Shibu, "K.V. Introduction to Embedded Systems", Tata McGraw Hill, 2009
2. Marilyn Wolf, "Computers as components: Principles of Embedded Computing System Design" Elsevier, 2012.

3. Raj Kamal, "Embedded systems Architecture, Programming and Design", 2nd Edition, 2008
4. Lyla B Das, "Embedded Systems: An Integrated Approach", Pearson, 2013
5. Robert Ashby, "Designer's Guide to the Cypress PSoC Newnes", An imprint of Elsevier, 2006.
6. Oliver H. Bailey, "The Beginner's Guide to PSoC Express" Timelines Industries Inc., 1st Edition, 2007.

M.Tech. – III Sem.

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(EC24DOE302) FOUNDATIONS OF ARTIFICIAL INTELLIGENCE

COURSE OBJECTIVES:
The objective of this course are to:
- Study the approaches to produce "intelligent" systems, Knowledge representation (bothsymbolic and neural network), search and machine learning.
- Learn the principles and fundamentals of designing AI programs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
CO 1: Learn the concepts of artificial intelligence
CO 2: Study problem solving techniques
CO 3: Understand the representation of knowledge and reasoning mechanism
CO 4: Learn to planning and decision making
CO 5: Study network models used for learning

UNIT I: (10 Periods)
Introduction to artificial Intelligence, problem solving as state space search, Uninformed search, heuristic search, informed search, constrained satisfaction problem.

UNIT II: (10 Periods)
Knowledge representation and Reasoning-Introduction to knowledge representation, propositional logic, first order logic, inference in first order logic, answer extraction, procedural control of reasoning, reasoning under uncertainty, Bayesian network, decision network.

UNIT III: (10 Periods)
Planning and decision making- Introduction to planning, plan space planning, planning graph and graph plan, practical planning and acting, sequential decision problems, making complex decisions.

UNIT IV: (8 Periods)
Machine learning- Introduction to ML, learning decision trees, linear regression, SVM, supervised learning, unsupervised learning, reinforcement learning,

UNIT V: (7 Periods)
Introduction to deep learning and neural network learning.

Total Periods: 45

TEXT BOOKS:
1. Patrick Henry Winston, Artificial Intelligence, Third Edition, Addison-Wesley Publishing Company, 2004.
2. Stuart Russell and Peter Norvig, Artificial Intelligence: A Modern Approach, 3rd Edition, PHI 2009.

REFERENCES:
1. Nils J Nilsson, Principles of Artificial Intelligence, Illustrated Reprint Edition, Springer Heidelberg, 2014.
2. Nils J. Nilsson, Quest for Artificial Intelligence, First Edition, CambridgeUniversity Press, 2010.

M.Tech. – III Sem.

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(EC24DOE303) INTRODUCTION TO INDUSTRY 4.0 AND INDUSTRIAL INTERNET OF THINGS

COURSE OBJECTIVES:

The objective of this course are to:

- Give the students an understanding of Industry 4.0 and Cyber security.
- Develop the skills for analyzing the industrial internet of things in industryto modify the various existing industrial systems.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand the basic concepts of communication networking
CO 2: Analyze the Business model and reference architecture
CO 3: Understand the globalization and emerging issues in industrial 4.0 and artificial intelligence, big data and advanced analysis
CO 4: Verify the design flow of industrial IoT
CO 5: Verify the process of synthesis and post-synthesis in various applicationsin Industrial IoT.

UNIT I: (10 Periods)

Introduction: Sensing & actuation, Communication-Part I, Part II, Networking- Part I, Part II, Industry 4.0: Globalization and Emerging Issues, The Fourth Revolution, LEAN Production Systems, Smart and Connected Business Perspective, Smart Factories, Industry 4.0: Cyber Physical Systems and Next Generation Sensors, Collaborative Platform and Product Lifecycle Management, Augmented Reality and Virtual Reality, Artificial Intelligence, Big Data and Advanced Analysis, Cybersecurity in Industry 4.0.

UNIT II: (8 Periods)

Basics of Industrial IoT: Industrial Processes-Part I, Part II, Industrial Sensing & Actuation, Industrial Internet Systems, IIoT - Introduction, Industrial IoT: Business Model and Reference Architecture: IIoT - Business Models-Part I, Part II, IIoT Reference Architecture-Part I, Part II, Industrial IoT- Layers: IIoT Sensing-Part I, Part II, IIoT Processing-Part I, Part II, IIoT Communication-Part I.

UNIT III: (10 Periods)

Industrial IoT- Layers: IIoT Communication-Part II, Part III, IIoT Networking- Part I, Part II, Part III, Industrial IoT: Big Data Analytics and Software Defined Networks: IIoT Analytics - Introduction, Machine Learning and Data Science - PartI, Part II, R and Julia Programming, Data Management with Hadoop, Industrial IoT: Big Data Analytics and Software Defined Networks: SDN in IIoT-Part I, Part II, Data Center Networks, Industrial IoT: Security and Fog Computing: Cloud Computing inIIoT-Part I, Part II.

UNIT IV: (10 Periods)

Industrial IoT: Security and Fog Computing - Fog Computing in IIoT, Security in IIoT-Part I, Part II, Industrial IoT- Application Domains: Factories and Assembly Line, Food Industry, Industrial IoT- Application Domains: Healthcare, Power Plants, Inventory Management & Quality Control, Plant Safety and Security (Including AR and VR safety applications), Facility Management, Industrial IoT- Application Domains: Oil, chemical and pharmaceutical industry, Applications of UAVs in Industries, Real case studies.

UNIT V: (7 Periods)

Case study: Milk Processing and Packaging Industries, Manufacturing Industries - Part I & II, Student Projects – Part I & II, Virtual Reality Lab, Case study - VII : Steel Technology Lab.

Total Periods: 45

TEXT BOOKS:

1. Alasdair Gilchrist "Industry 4.0: The Industrial Internet of Things", A press, Springer, New York, 2016.

REFERENCES:

1. Sabina Jeschke, Christian Brecher, Housing Song, and Danda B. Rawat "Industrial Internet of Things: Cyber manufacturing Systems" Springer International Publishing Switzerland, 2017.

M.Tech. – III Sem.

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(EC24DOE304) NATURAL LANGUAGE PROCESSING

COURSE OBJECTIVES:

The objective of this course are to:

- Understand NLP tasks in syntax, semantics and pragmatics
- Implement machine learning techniques used in NLP

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO 1: Understand NLP and the role of machine learning in NLP
CO 2: Describe finite state transducer operations and pronunciation modelling inNLP
CO 3: Illustrate various probabilistic models in NLP.
CO 4: Study semantic analysis in NLP
CO 5: Learn various machine translation approaches and the different evaluation metrics.

UNIT I: **(10 Periods)**

Introduction – Why NLP? NLP versus speech recognition- Applications-problem ofambiguity-role of machine learning in NLP- Basic neural networks for NLP.

UNIT II: **(7 Periods)**

Words – Morphology and Finite State Transducers-Tokenization – ComputationalPhonology and Pronunciation Modelling.

UNIT III: **(10 Periods)**

Probabilistic models in NLP — Role of language models- Simple N-gram model – Evaluation: Perplexity and Word Error Rate. Parts of Speech Tagging- HiddenMarkov models– Viterbi algorithm, Maximum Entropy Markov model.

UNIT IV: **(10 Periods)**

Semantic analysis - Lexical semantics and word-sense disambiguation. Compositional semantics. Semantic Role Labeling and Semantic Parsing.

UNIT V: **(8 Periods)**

Machine Translation - Statistical translation, word alignment, phrase-based translation, and synchronous grammars, evaluation.

Total Periods: 45

TEXT BOOKS:

1. Natural Language Processing, by Jacob Eisenstein, MIT Press.
2. Speech and Language Processing by Daniel Jurafsky and James H. Martin

REFERENCES:

1. Foundations of Statistical Natural Language processing by Manning C.D and Schutze, First Edition, MIT Press, 1999
2. Neural Network Methods for Natural Language Processing by Yoav Goldberg, Morgan and Claypool Publishers.